Vertically Integrated Processor and Memory Module Design for Vector Supercomputers

Background and Motivation

Vector Supercomputers

- Powerfull core and high memory bandwidth introduce a well-balanced Byte/Flop(B/F) rate.

Trends of mem. BW per processor

High-memory bandwidth to keep a high Byte/Flop rate is mandatory for high sustained performance

Expensive Memory Bandwidth

On-chip area occupancy

Power breakdown of nodes (Momose et al. @SC10)

Interfaces for off-chip memory accesses consume a huge amount of area and power

Designing Vertically Integrated Processor and Memory Modules

Potentials of Vertical Integration

- 2.5D integration
  - Integrating multiple dies on a Si-interposer
  - Improving inter-die bandwidth per power compared to PCB (printed circuit board)

Comparing wires on PCB and Si-interposer

Comparing the lengths of the interconnections between PCB and Si-interposer reveals that the lengths of the interconnections become shorter than those of PCB!

Module Design using Vertical Integration

- The current vector supercomputer
  - CPU x15
  - Clissibar Interconnect
  - HUB x312
  - RAM x12,288
  - FV x1

Compact modules using vertical integration

- PCB implementation
  - CPU
  - Mem. Module
  - SerDes

2.5D implementation

- The lengths of the interconnections become shorter than those of PCB!

2.5D (Si-interposer) + 3D (memory) = 5.5D (module)!

Comparing the lengths of the interconnections between PCB and Si-interposer reveals that the lengths of the interconnections become shorter than those of PCB!

To realize a high energy efficiency, computing nodes should be as compact as possible

Conclusions

- 2.5D implemented nodes of vector supercomputers significantly benefit in power reduction.

Future work: More detailed evaluations for design space explorations considering cost, power, and thermal parameters.

Both of the implementations achieve similar performances.

The energy consumed in Mem I/F is significantly reduced.

The implementations of Si-interposers achieve significant energy reductions.

The memory system already provides enough B/F ratio.

Evaluations

Experimental Setup

Simulators

- NEC SX Simulator and CACTI 6.5

Simulation parameters

- Network of Workstations
- Interconnect
- Core
- Memory
- Power

- Benchmarks

- Various: Single-core performance
- SIM: Inter-processor communication

Results

Performance

Energy consumption and its breakdown

- Mem I/F
- DRAM read
- DRAM write
- DRAM static

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The implementations of Si-interposers achieve significant energy reductions.

The energy consumed in Mem I/F is significantly reduced.

The memory system already provides enough B/F ratio.

The SerDes logic in the PCB implementations can be eliminated by the Si interposer implementations.